

Client's ref.: 91178  
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## TITLE

### METHOD OF FORMING BIT LINE CONTACT

#### BACKGROUND OF THE INVENTION

##### Field of the Invention

5       The present invention relates in general to a method of forming a contact structure. In particular, the present invention relates to a method of forming a bit line contact structure comprising a polysilicon spacer and a silicon nitride liner.

##### 10   Description of the Related Art

As ICs become more compact, semiconductor design has reduced device dimensions. For example, 64M DRAM process has shifted from 0.35 $\mu$ m to 0.3 $\mu$ m or less, and 128M or 256M DRAM process to less than 0.2 $\mu$ m.

15       Self-aligned contact (SAC) process is often used to enhance conducting wire accuracy, but becomes more difficult as critical dimension (CD) reduces. For example, in filling processes of bit line contact with line width lower than 0.11 $\mu$ m, the above mentioned bit line contact is lower than  
20   0.038 $\mu$ m of exposed drain area width, easily suffering bit line contact from open circuits or word-line/bit-line from short circuits when a conductive layer is formed, functions may be disabled, impacting product yield and cost.

FIGS. 1A~1F show conventional self-aligned contact  
25   fabrication method resulting in bit line open circuits or word-line/bit-line short circuits.

Client's ref.: 91178  
Our ref: 0548-9210us/final/yyhsu/Kevin

First, FIG. 1A shows a substrate 10 having a transistor structure, an alternating arrangement of the drain 12/source 14 areas on the active area surface of substrate 10, with a gate electrode 20 between source 14 and drain 12 areas protruding from substrate 10. Gate electrode 20 has a multi-layer structure to meet several requirements, having a gate dielectric layer 21, a conductive layer 22, a metal silicide layer 23, and a hard mask layer 24. A silicon nitride spacer 25 is formed on the sidewalls of the gate electrode 20. With spacer 25 on the sidewalls of the gate electrode 20, the exposed drain area 12 widths between the adjacent spacers of the gate electrodes 20 are less than 0.038 $\mu$ m if line width is minimized to about 0.11 $\mu$ m.

Subsequently, a dielectric layer 30 and a photoresist pattern layer 60 are formed on substrate 10. In FIG. 1B, the photoresist pattern layer 60 has an open region 60a acting as subsequent bit line contact position.

Next, the exposed dielectric layer 30 on the open region 60a is removed, forming a dielectric layer contact when the bit line contact is exposed from drain area 12, and a conductive layer 22 is filled into the above mentioned dielectric layer contact acting as the bit line contact plug. FIGS. 1C~1D show bit line contact occurring, resulting in open circuits. FIGS. 1E~1F show word-line/bit-line occurring, resulting in short circuits.

FIG. 1C shows an etching mask using photoresist pattern layer 60, wherein the dielectric layer 30 is anisotropically etched and forms the dielectric contact 31 exposed from the drain area 12, the bit line contact. Nevertheless, as mentioned above, the exposed drain area 12 width is less

Client's ref.: 91178  
Our ref: 0548-9210us/final/yyhsu/Kevin

than 0.038 $\mu$ m only with line width as low as 0.11 $\mu$ m, in addition, the dielectric contact 31 is deep, such that etching of the dielectric layer 30 at the bottom of the dielectric contact 31 is more difficult when the dielectric  
5 layer 30 is close to the drain areas 12. After the above anisotropic etching, the incompletely or unetched dielectric layer 30 normally remains at the dielectric contact 31 bottom, resulting in the drain areas 12 not being exposed.

In FIG. 1D, barrier layer 40 is formed within the  
10 dielectric contact 31, and a conductive layer 50 is filled to act as bit line connection, when the dielectric layer 30 is not a conductor, such that conductive layer 50 and drain areas 12 are not electrically connected, resulting in the described bit line contact open circuits.

15 In order to prevent open circuits, a conventional method uses a lower etching selectivity of self-aligned contact (SAC) process parameters to perform the contact etching process, however, in the process designs of forming the bit line contact, in order to prevent short circuits  
20 between the gate electrode 20 (as the bit line) and subsequent bit line, in the gate electrode 20, the conductive polysilicon layer 22 and the metal silicide layer 23 are protected by hard mask layer 24 and sidewall spacer 25, then etched by high etching selectivity method to  
25 prevent their being exposed and connecting to subsequent bit line, with resulting short circuits. However, as etching selectivity for removal of the dielectric layer 30 located at bottom of the dielectric window 31a decreases, not only is the dielectric window 31a width increased, but also a  
30 portion of the hard mask 24 and spacer 25 is removed,

Client's ref.: 91178  
Our ref: 0548-9210us/final/yyhsu/Kevin

forming the spacer 25a, exposing metal silicide layer 23, or even polysilicon layer 22.

FIG. 1F, when the conductive metal silicide layer 23 of the gate electrode 20 is exposed, once a barrier layer 40 is formed on the dielectric contact 31', and the conductive layer 50 is filled to connect with the bit line, the conductive layer 50 and the metal silicide layer 23 become electrically connected, resulting in the mentioned bit-line/word-line short circuits.

In conventional implementation, overetching is also utilized to prevent bit line contact from short circuits, however, during formation of bit line contact, the silicon nitride is generally employed as a hard mask 24 and sidewall spacer 25, with the silicon oxide as dielectric layer 30, such that etching selectivity of dielectric layer 30 to hard mask 24 and sidewall spacer 25 is around 10. Even so, such low etching selectivity also etches hard mask 24 and sidewall spacer 25, exposing polysilicon layer 22 and the metal silicide layer 23, resulting in word- line/bit-line short circuits.

#### SUMMARY OF THE INVENTION

Accordingly, an object of the invention is to provide a method of forming bit line contact using barrier material with high etching selectivity as a spacer, whereby self-aligned bit line contact etching is performed. Bit line contact open circuits and word-line/bit-line short circuits are prevented when the subsequent conductive layer is filled into the bit line contact.

Client's ref.: 91178  
Our ref: 0548-9210us/final/yyhsu/Kevin

In order to achieve the above object, the invention provides a method of forming bit line contact, comprising providing a substrate having a plurality of transistors therein, each including a gate electrode and doping areas  
5 serving as drain and source, forming a pair of barrier spacers on the opposite sidewalls of the adjacent gate electrodes, forming a dielectric layer overlying the surface of the gate electrodes, barrier spacers and doping areas, and, using the barrier spacer and the doping areas as etch  
10 stop, etching a portion of the dielectric layer to form a bit line contact.

In the above method, the barrier spacer may be formed by a conformal barrier layer on the surface of the gate electrodes and the doping areas, followed by etching the  
15 barrier layer, such that the barrier layer forms a barrier spacer on the sidewalls of the gate electrodes, forming a mask layer to cover the retained barrier spacer, and removing the unmasked portion of the barrier spacer.

In the above method, before forming the dielectric  
20 layer, a liner layer may be formed on the surface of the gate electrodes, barrier spacers and doping areas.

The invention provides another method of forming bit line contact comprising providing a substrate having a plurality of transistors therein, each including a gate  
25 electrode and doping areas serving as drain and source, forming a polysilicon spacer on the sidewalls of the gate electrode, forming a mask layer to cover a portion of the polysilicon spacer and removing the unmasked portion of the polysilicon spacer, removing the mask layer and forming a  
30 dielectric layer on the surface of the gate electrodes, the

Client's ref.: 91178  
Our ref: 0548-9210us/final/yyhsu/Kevin

polysilicon spacers and the doping areas, and, using the polysilicon spacer and the substrate as etch stop, etching a portion of the dielectric layer to form a bit line contact.

5 In this method, the polysilicon spacer may be formed by a conformal polysilicon layer on the surface of the gate electrodes and doping areas and anisotropically etching the polysilicon layer so that the remaining polysilicon layer forms a polysilicon spacer on the sidewalls of the gate electrode.

10 In the above method, before forming the dielectric layer, a liner layer may be formed on the surface of the gate electrodes, polysilicon spacers and doping areas.

The above objects are further accomplished by a method of forming bit line contact comprising providing a substrate  
15 having a plurality of transistors therein, each including a gate electrode and doping areas serving as drain and source, forming a conformal polysilicon layer on the surface of the gate electrodes and doping areas, anisotropically etching the polysilicon layer so that the remaining polysilicon  
20 layer forms a polysilicon spacer on the sidewalls of the gate electrode, forming a mask layer on the surface of adjacent gate electrode doping area and a portion of the gate electrode located on both sides of the doping area, removing the mask layer and forming a liner layer overlying  
25 the surface of the gate electrodes, polysilicon spacers and doping areas, forming a dielectric layer on the liner layer, using the polysilicon spacer and the doping area as an etch stop, etching a portion of the dielectric layer and the liner layer to form a bit line contact, and filling a

Client's ref.: 91178  
Our ref: 0548-9210us/final/yyhsu/Kevin

conductive layer into the bit line contact to act as a bit line contact plug.

#### DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention,  
5 reference is made to a detailed description to act as read in conjunction with the accompanying drawings, in which:

FIG. 1A~1F are cross sections showing fabrication of the conventional bit line contact.

FIG. 2A~2I are cross sections of the method of forming  
10 a bit line contact according to the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

In FIG. 2A, a semiconductor substrate 100, such as a single crystal silicon substrate, is provided with a transistor structure thereon. The active region of the  
15 substrate 100 has doping area 110 comprising drain and source areas. Between doping areas 110, gate electrodes 120a~120d protrude from substrate 100. The gate electrode is a bit line, having multi-layer structure as in the gate electrode 120a~120d of FIG. 2A, including gate dielectric  
20 layer 121, such as an oxide layer, polysilicon layer 122 as a conductive layer, metal silicide layer 123 as a conductive layer, such as Tungsten silicide, and hard mask layer 124, such as a silicon nitride layer. Sidewalls of the gate electrode 120a~120d have a silicon nitride spacer 125. The  
25 gate electrode structures are examples, not intended to limit the scope of the invention.

FIG. 2B shows a barrier layer is formed on the surface of the substrate 100, especially spacers 125, doping areas

Client's ref.: 91178  
Our ref: 0548-9210us/final/yyhsu/Kevin

110, and gate electrodes 120a-120d, such that gate electrodes are fully covered. The barrier layer can have barrier properties, such as conductive or semiconductor materials, or comprise combinations thereof, such as  
5 polysilicon layer 130, formed by, for example low pressure chemical vapor deposition (LPCVD), with reaction gases of PH<sub>3</sub>, SiH<sub>4</sub> and N<sub>2</sub> or AsH<sub>3</sub>, SiH<sub>4</sub> and N<sub>2</sub>, at between 500~650°C, and ion concentration between 1E20 and 1E21 atom/cm<sup>3</sup>.

Next, in FIG. 2C, polysilicon layer 130 is etched,  
10 forming a polysilicon spacer 132 on the sidewalls of the gate electrode 125, level with gates 120a~120d. Polysilicon layer 130 can be etched using, for example, magnetic enhanced reactive ion (MERIE), electron cyclotron resonance plasma (ECR) or reactive ion etching (RIE), with gases  
15 including, for example, SF<sub>6</sub>, O<sub>2</sub>, Cl<sub>2</sub> and HBr.

Next, a portion of the retained polysilicon spacer 132 is formed using photoresist layer 140 as a mask layer. FIG. 2D shows a photoresist pattern layer 140 on the doping area 110 between the gate electrodes 120b and 120c, whereby a  
20 portion of the surface of the gate electrodes 120b and 120c is formed. This step masks the polysilicon spacer 132 on both sides of the gate electrodes 120b and 120c in the desired bit line contact position. A photoresist pattern layer 140 is formed to protect the masked polysilicon spacer  
25 132 from removal during subsequent polysilicon spacer 132 etching.

Using the photoresist pattern layer 140 as a mask, the portion of the unmasked polysilicon spacer 132 located on both sides of the gate electrodes 120a and 120d and a  
30 portion of electrodes 120b and 120c unmasked by photoresist

pattern layer 140 are etched. Then, photoresist pattern layer 140 is removed using solvent or plasma etching, leaving polysilicon spacer 132 between the gate electrodes 120b and 120c. At this point, the high dielectric etching selectivity polysilicon acts as the gate electrode spacer. Wet etching of polysilicon spacer 132, such as BOE or KOH, can remove unmasked polysilicon spacer 132 from photoresist pattern layer 140.

In FIG. 2F, a conformal liner layer 150 is deposited on the substrate surface 100, the gate electrode sidewalls, and the doping areas 110 using, for example, chemical vapor deposition (CVD) with SiON, SiN or SiO<sub>2</sub>, at thickness from 20 to 200Å. Then, in FIG. 2G, CVD deposits a dielectric layer 160 over liner layer 150. After formation of the dielectric layer 160, dielectric layer 160 can be planarized using CMP or etching back, and unwanted dielectric layer is removed. Dielectric layer 160 can be boro-phosphosilicate glass (BPSG), high density plasma chemical vapor deposition (HDPCVD) oxide, oxygen-containing silicate, or combinations thereof.

In FIG. 2H, a photoresist pattern layer on the dielectric layer 160 is formed as an etching mask. Self-aligned contact (SAC) etching is performed using the polysilicon spacer 132, the gate electrode hard mask layer 124, and the substrate 100 as an etch stop. The dielectric layer 160 and the liner layer 150 are etched on the gate electrode 120b and 120c, forming a bit line contact 180. SAC bit line contact can use anisotropic etching, such as magnetic enhanced reactive ion (MERIE), electron cyclotron resonance plasma (ECR), or reactive ion etching (RIE).

Client's ref.: 91178  
Our ref: 0548-9210us/final/yyhsu/Kevin

The invention provides bit line contact formation using a barrier spacer for the SAC protection layer, for example, polysilicon, having high etching selectivity of 50 or more. With such high etching selectivity, the barrier spacer is not easily removed, and the width of dielectric contact 180 does not increase, such that the portion of the hard mask layer 124 and the sidewall spacer 125 are also not exposed during etching. Thus bit line contact open circuits or bit line/word-line short circuits do not occur when subsequent conductive layer 170 is filled into the bit line contact. Semiconductor process yield is enhanced and process costs are reduced.

Although the present invention has been particularly shown and described above with reference to the preferred embodiment, it is anticipated that alterations and modifications thereof will no doubt become apparent to those skilled in the art. It is therefore intended that the following claims be interpreted as covering all such alteration and modifications as fall within the true spirit and scope of the present invention.